



# ‘The DØ Run 2b Silicon Tracker Project’

## Status Report

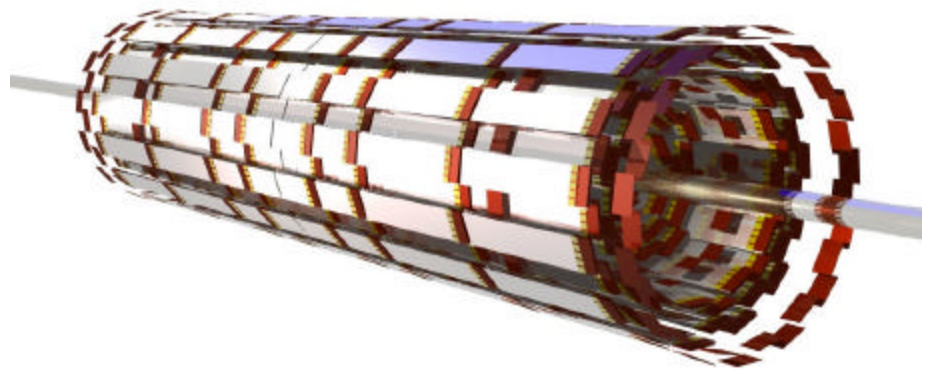
DØ Beaune Workshop  
June 15-20, 2003

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Fermilab

For the Run 2b Silicon Group

# Outline

- ❑ Reminder of Design of the Silicon Detector
- ❑ Status of design and prototyping
  - ◆ Sensors
    - Outer Layers
    - Inner Layers
  - ◆ Support Structures
    - Layer 0
    - Layer 1
  - ◆ Modules, Staves
  - ◆ Readout System
    - SVX4
    - cables
    - boards
    - ...
- ❑ Testing status
- ❑ Software
- ❑ Schedule
- ❑ Summary and Conclusions



# Detector Design

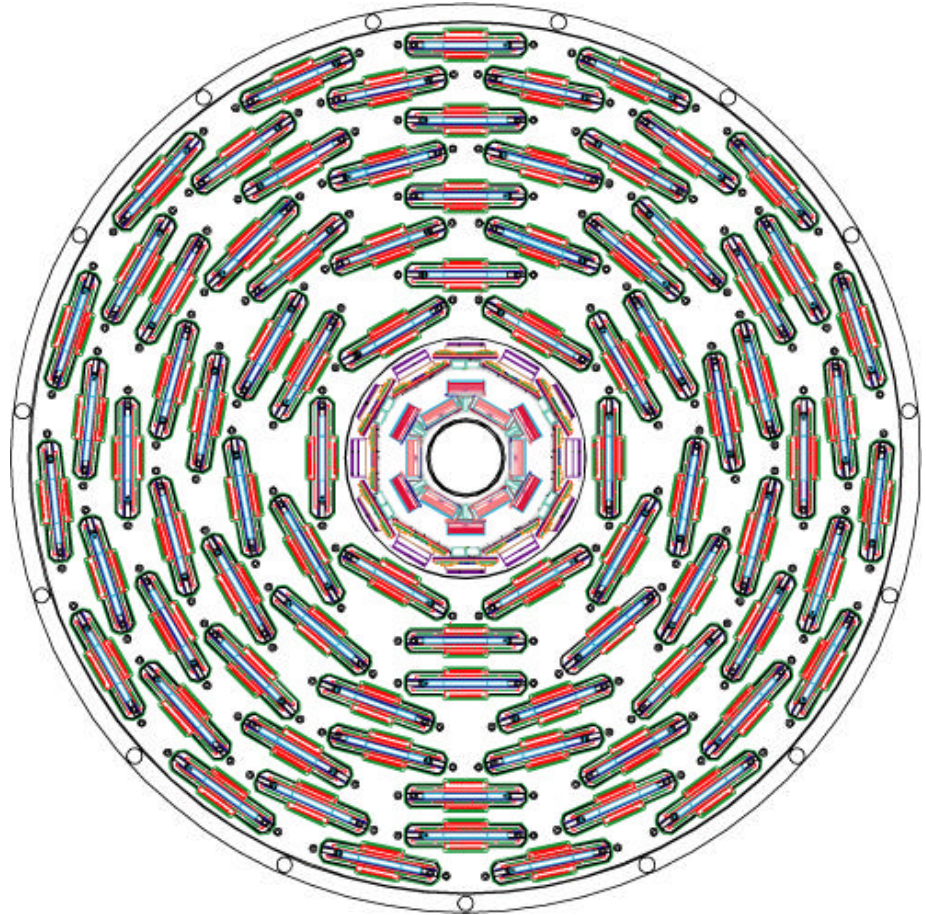
## ❑ Six layer silicon tracker, divided in two radial groups

- ◆ Inner layers: Layers 0 and 1
  - $18\text{mm} < R < 39\text{mm}$
  - Axial readout only
  - 50/58  $\mu\text{m}$  readout for L0/L1
  - Assembled into one unit
  - Mounted on integrated support
- ◆ Outer layers: Layers 2-5
  - $53\text{mm} < R < 164\text{ mm}$
  - Axial and stereo readout
  - 60  $\mu\text{m}$  readout
  - Stave support structure
- ◆ All sensors intermediate strips

## ❑ Employ single sided silicon only, 3 sensor types, axial strips,

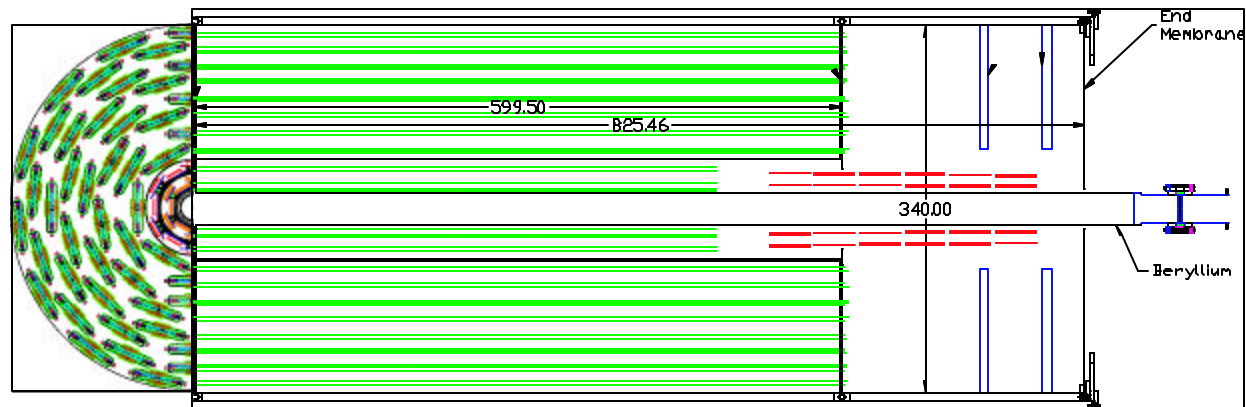
- ◆ 2-chip wide for Layer 0
- ◆ 3-chip wide for Layer 1
- ◆ 5-chip wide for Layers 2-5

## ❑ No element supported from the beampipe



# From Basics to Details

- ❑ Status will be presented of nearly every element of the detector following the signal path
  - ◆ Sensors
  - ◆ Support Structures
  - ◆ Hybrids
  - ◆ Downstream Electronics



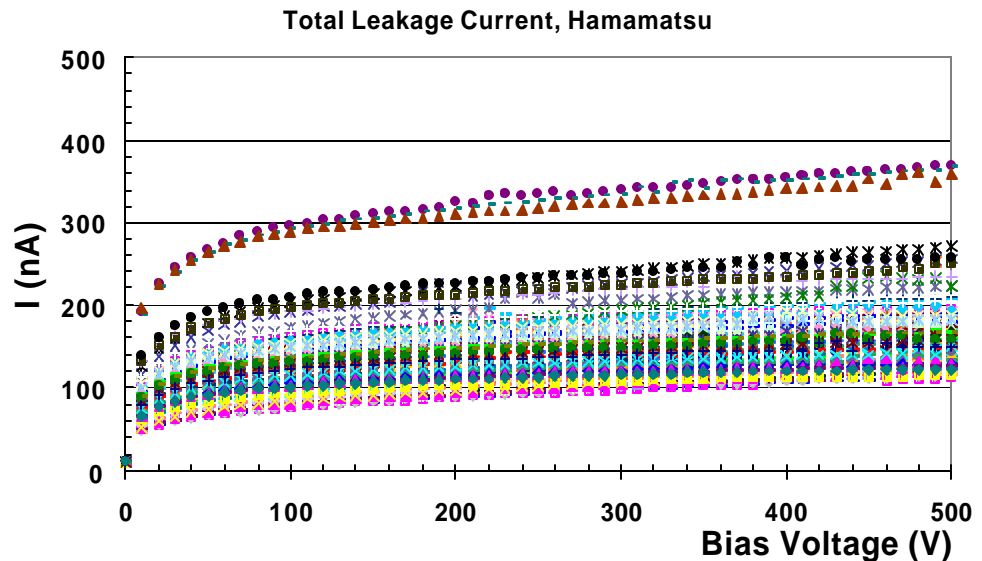
# Outer Layer Sensors

## □ Layers 2-5

- ◆ 5-chip wide, 60μm pitch, intermediate strips, 40.34x100 mm cut dimension
- ◆ Order placed for 100 prototype sensors, May '02; sensors shipped Nov. 29
- ◆ Hamamatsu's internal QA program indicates sensors are of very high quality

### - Bulk tests

- No single sensor exceeding leakage current of 400 nA



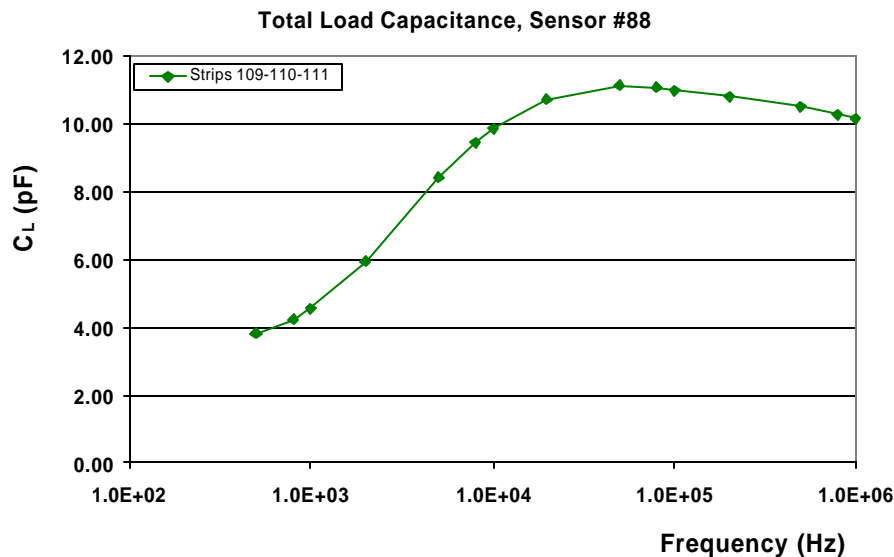
### - Strip tests

- Only three sensors have a total of 8 strip defects

Lot No.	Serial No.	Type	Ch. No.
SWA61737	51	AC-AL short	20-21
		AC-AL short	52-53
SWA61737	65	AC-AL short	39-40
SWA61738	108	Coupling short	94
		Coupling short	95

# Outer Layer Sensors

- ◆ Subset of sensors undergone full QA program
  - I-V curve, up to bias voltage of 700V; C-V curve, determination  $V_{\text{depl}}$
  - Long-term stability of detector total leakage current
  - AC- and DC scan
  - Resistance of implant, poly-silicon and Aluminization
  - Interstrip capacitance and total load capacitance



Total load capacitance  
 $C_L \sim 1\text{pF/cm}$  for frequencies  
of interest

- ◆ Sensors satisfy all electrical specifications
  - All HPK defects reproduced; very few (~5) additional defects uncovered

# Outer Layer Sensors Status

- ❑ Production Readiness Review March 6,7 at Fermilab
  - ◆ Review very helpful and uncovered some QA issues which have been addressed
- ❑ Full production order for 2735 sensors placed with Hamamatsu mid April
  - ◆ HPK delivery schedule
    - 130 pcs            during July, 2003
    - 130 pcs            during Aug., 2003
    - 270 pcs            during Sep., 2003
    - 270 pcs            during Oct., 2003
    - 270 pcs            during Nov., 2003
    - 270 pcs            during Dec., 2003
    - 270 pcs            during Jan., 2004
    - 270 pcs            during Feb., 2004
    - 400 pcs            during Mar., 2004
    - 400 pcs            during Apr., 2004
    - 55 pcs             during May, 2004

# Layer 1 Sensors

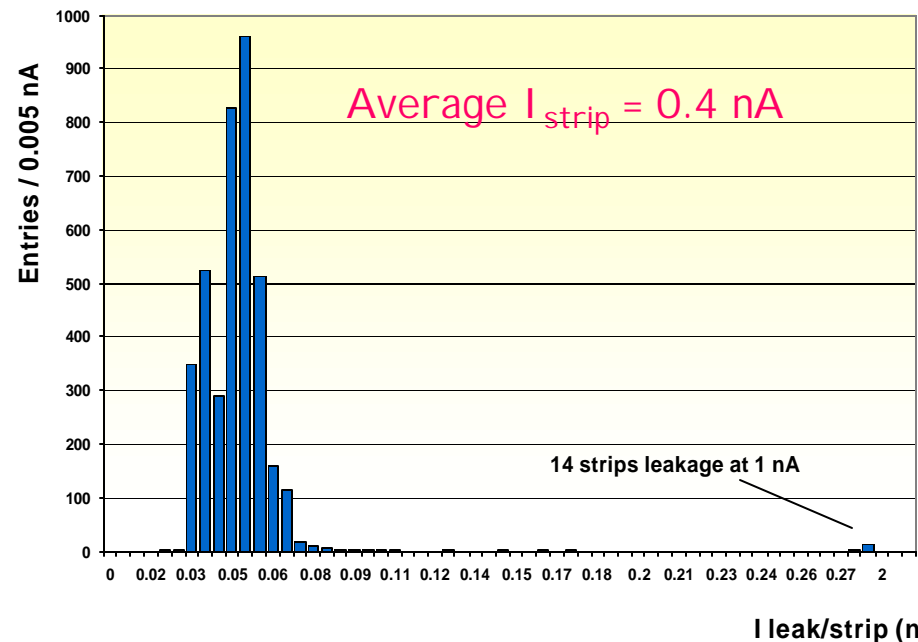
## □ Layer 1

- ◆ 3-chip wide, 58 $\mu$ m pitch, intermediate strips, 24.3x79.4 mm cut dimension
- ◆ Order placed for 10 prototype sensors, April '02; sensors shipped Sept. 21
- ◆ Hamamatsu's internal QA program indicates sensors are of good quality

Lot No.	Serial No.	Type	Ch. No.
SWA61589	6	Coupling short	267
SWA61589	7	Coupling short	320
SWA61589	20	AC-AL open	47
		AC-AL open	48

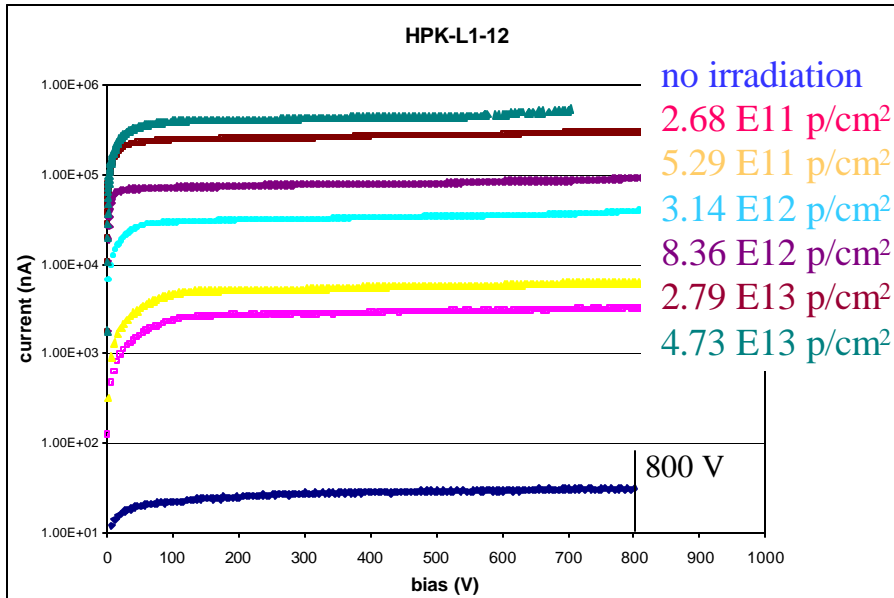
– four defective channels for three sensors

- ◆ strip leakage current for all 10 sensors at FDV
  - average strip current of 0.4 nA
  - 14 strips have a current of 1 nA
  - specification:  $I_{\text{strip}} < 10$  nA
- ◆ PRR planned in July



# Layer 1 Sensors, Irradiation

- Exposed sensors and test structures to 10 MeV p beam at KSU
  - ◆ Mapped out depletion voltage and  $I_{\text{leak}}$  dependence as function of fluence

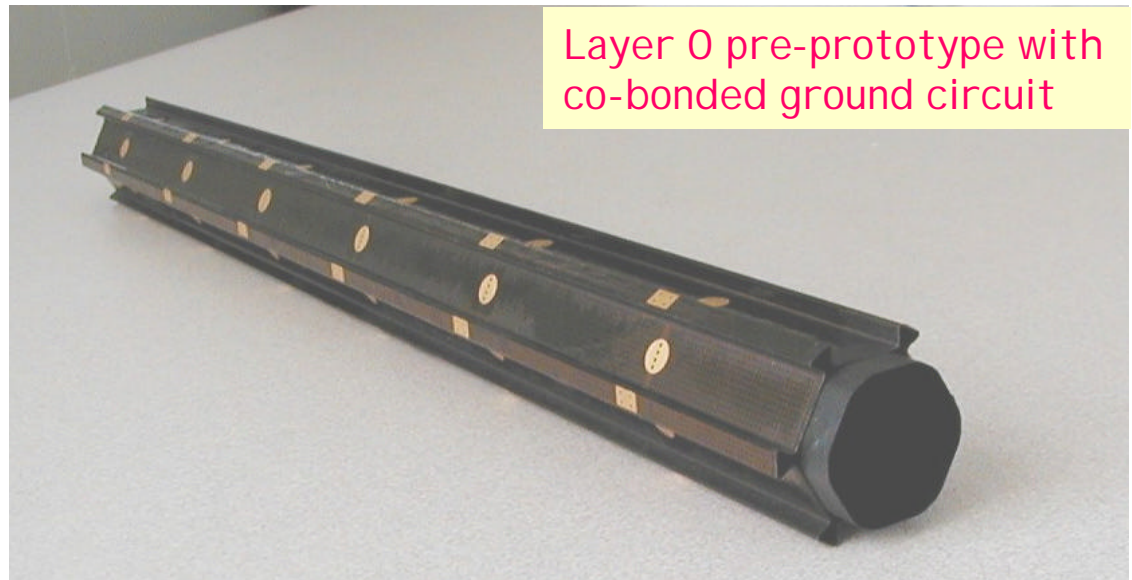
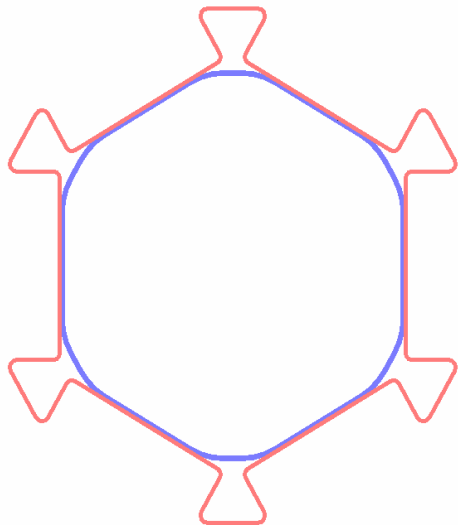


- ◆ No breakdown observed up to  $V_{\text{bias}} = 800$  V
- ◆  $I_{\text{leak}} \sim 300 \mu\text{A}$  at highest fluence
- ◆  $V_{\text{depl}}$  agrees with Hamburg model
- ◆ Data in agreement with other measurements (Montreal)

- Cross calibrated Faraday Cup fluence measurement with Cu foil activation
  - ◆ Independently verified at Fermilab
- All studies completed; PRR for inner layer sensors to take place, tentatively, end of July

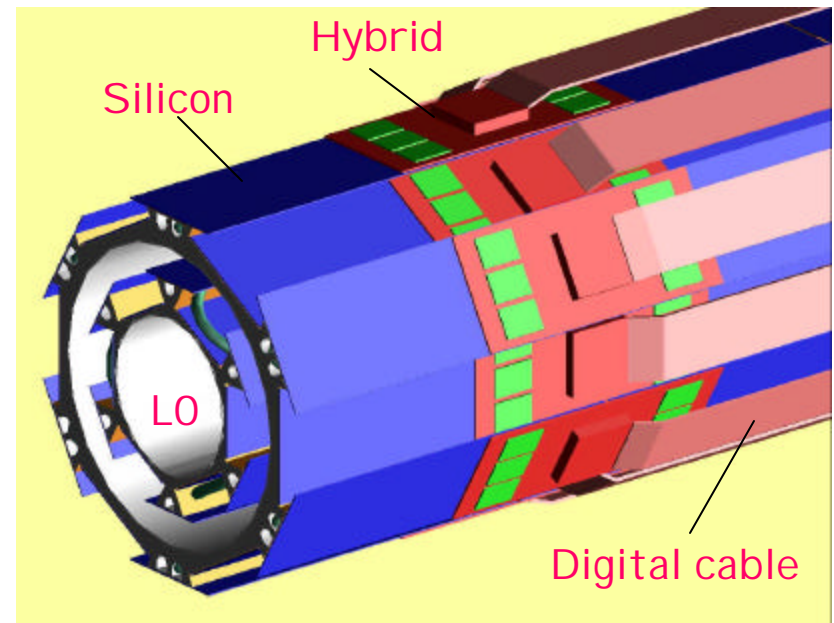
# Layer 0 Support Structure

- ❑ Inner shell, carbon fiber
  - ◆ 12-sided
  - ◆ 4 layers  $[0,90]_s$  lay-up
    - Cured thickness =  $0.22 \pm 0.01$  mm
- ❑ Outer shell, carbon fiber
  - ◆ 12-fold crenellated geometry
  - ◆ 6 layers  $[0,20,-20]_s$  lay-up
    - Cured thickness =  $0.31 \pm 0.01$  mm
  - ◆ No hybrids mounted on sensors for L0: analogue cables
- ❑ All FEA analyses, mechanical and thermal, completed
- ❑ All L0 and L1 prototype fabrication tooling completed and evaluated
  - ◆ deflection  $\sim 5 \mu\text{m}$  under applied load of 400 grams (distributed 200gr nominal load)
- ❑ Certified fabrication procedures for L0 prototype production by making pre-prototypes



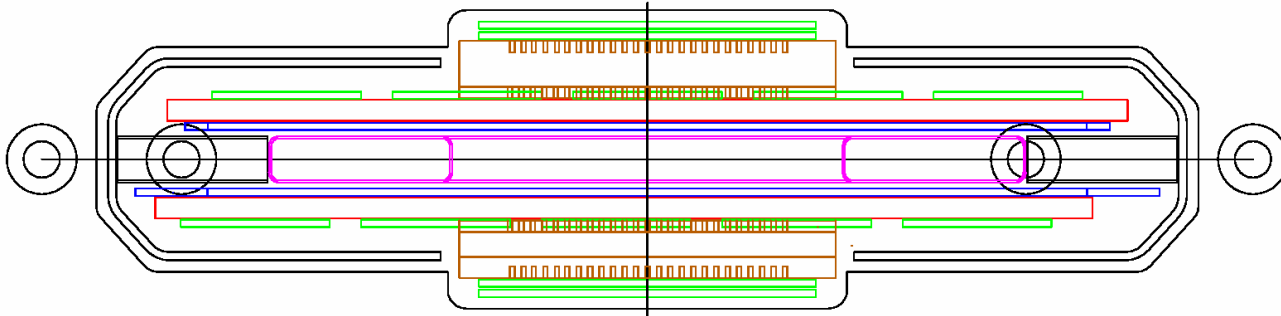
# Layer 1 Support Structure

- ❑ Support structure similar to Layer 0
- ❑ Readout electronics mounted on the sensors:
  - ◆ Power dissipation of 0.5W/chip
  - ◆ Power dissipation of  $< 0.1 \text{ W/sensor}$  after  $15 \text{ fb}^{-1}$
- ❑ Pre-prototypes made of all L1 components
  - ◆ Inner tube and castellated structure
  - ◆ Cooling manifold components machined and connectors to cooling tubes
  - ◆ Connection and support membranes



# Layers 2-5: Staves

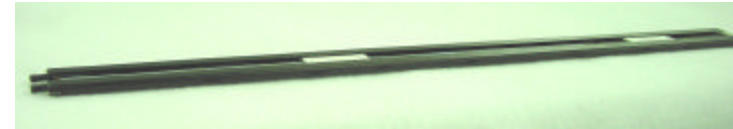
- Basic building block of the outer layers is a stave



- Stave is:
  - ◆ two-layer structure of silicon sensors
  - ◆ One layer of axial only, and one layer of stereo only readout
    - stereo angle obtained by rotating the sensor
  - ◆ Layers separated by a "core" with positioning and reference pins and PEEK cooling tubes
  - ◆ Total of 168 staves
- C-shells at edge of stave provide stiffness
- Staves are positioned and supported in carbon fiber bulkheads at  $z = 0$  and  $z = 605$  mm.
  - ◆ Locating features on stave provide the alignment

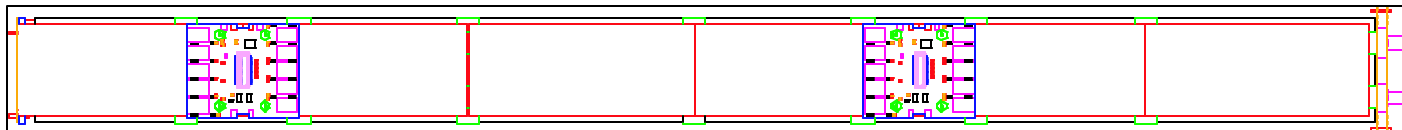
# Mechanical Stave and Bulkhead

- Met milestone for mechanical stave fabrication Dec 18, 2002
  - ◆ Measurements and procedures being developed for production and QA
    - Stave core thickness
    - Robustness of stave core through temperature cycles
    - C-channel deflection and twist
    - Thermal performance with dummy hybrids
    - Stave flatness after module installation
    - Stave deflection creep
    - Silicon deflection under negative pressure (-5 psig)
    - Forming of PEEK cooling tubes and leak tightness
      - tube, glue joint tube-nozzle, glue joint nozzle cilran tube
    - Reference pinholders and alignment tolerances
    - Ongoing leak test of PEEK tubes
  - ◆ No outstanding issues with staves; PRR in August
- Bulkhead
  - ◆ Measurements
    - Deflection to transverse and radial load
    - Placement of locating rings, now to few micron accuracy employing CMM as pick and place machine

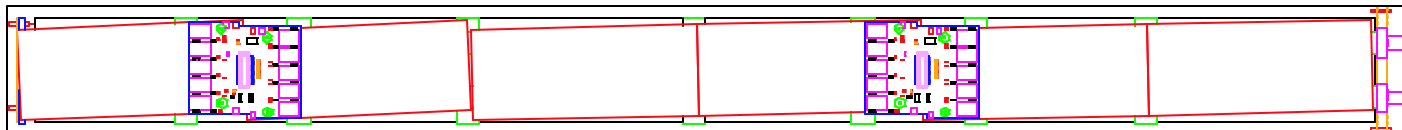


# Readout Modules

- ❑ Each stave has four readout modules
- ❑ Readout module length varies with z-position.
  - ◆ For all layers, the modules closest to  $z = 0$  are 200 mm long
  - ◆ Those furthest from  $z = 0$  are 400 mm long
- ❑ Four Readout module types
  - ◆ 10-10 (axial, stereo)
  - ◆ 20-20 (axial, stereo)
  - ◆ Ganged sensors will have traces aligned (sensors are 10cm long)
- ❑ Module configuration



Axial



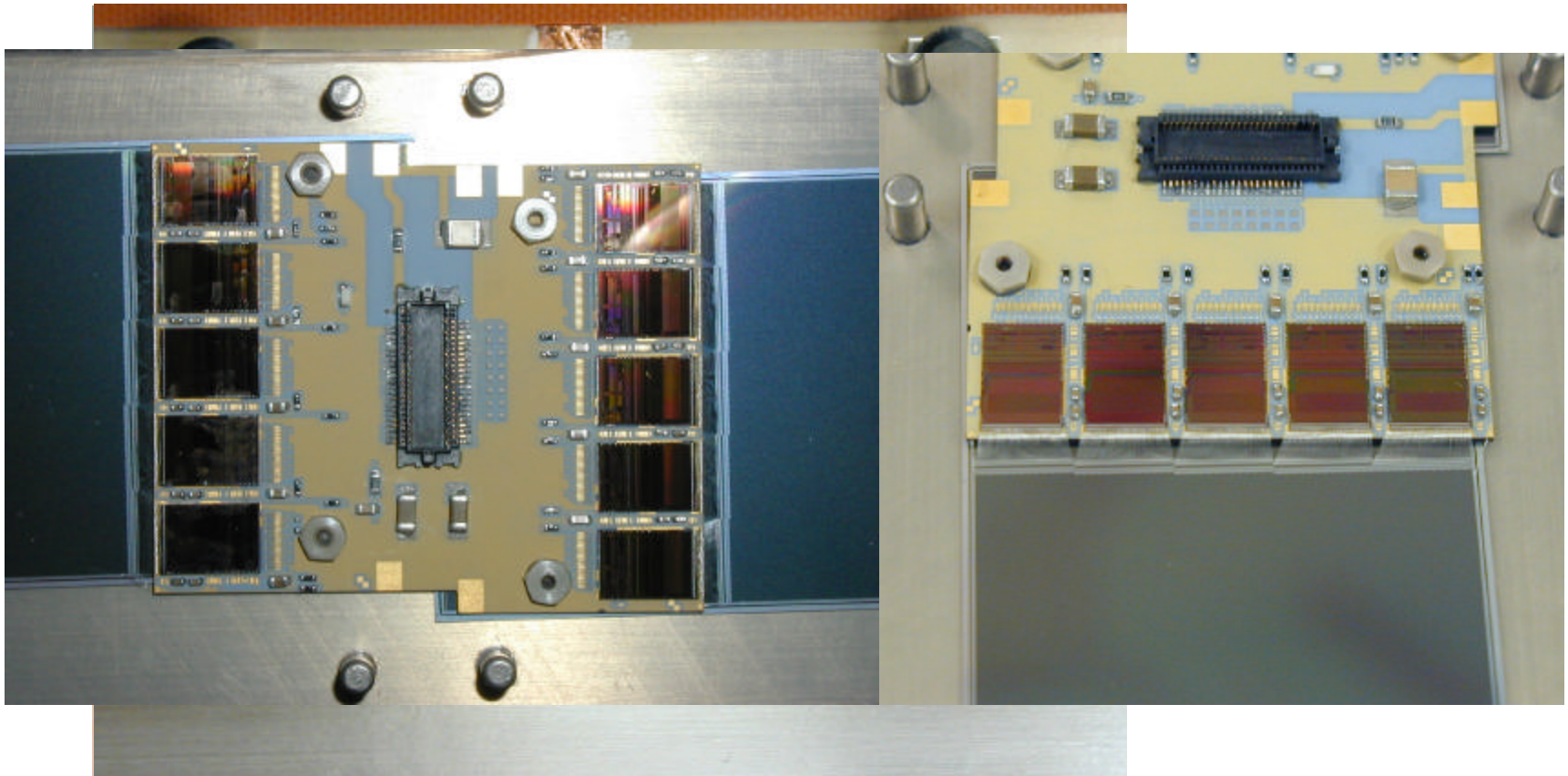
Stereo

$z=0$

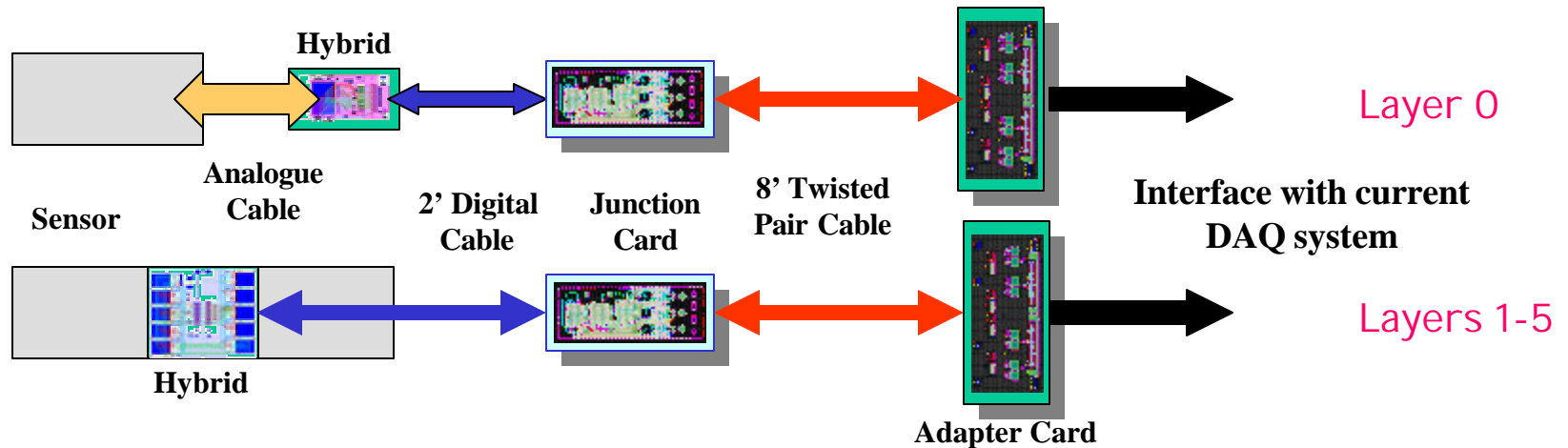
- ❑ Each readout module serviced by double-ended hybrid
  - ◆ Each hybrid has two independent readout segments

# Readout Module Fabrication

- ❑ Prototypes built of all six different readout modules
  - ◆ Prototype fixtures available for modules production for all types
    - Some fixtures are adequate and will be used for production
    - Fixtures for Layer 1 modules similar to 10-10 modules
  - ◆ Stave assembly fixtures and C-channel attachment fixtures are also prototyped



# Readout Schematics

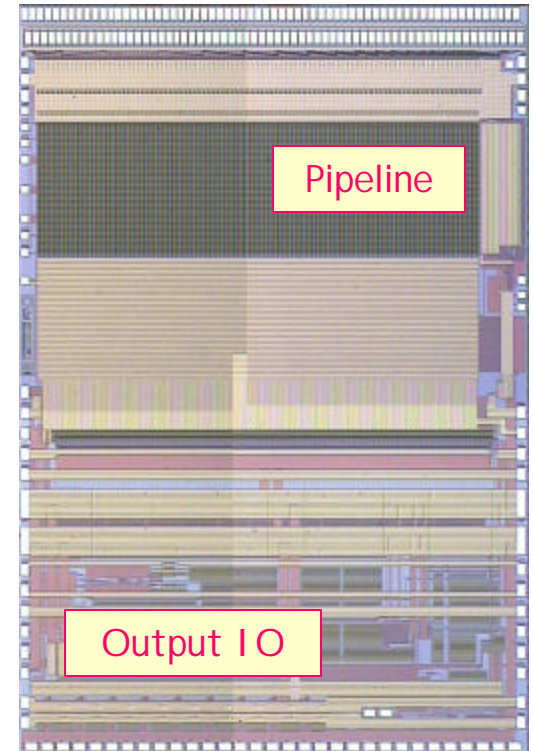


- ❑ Layers 1-5: Hybrids mounted on silicon
  - ◆ Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- ❑ Layer 0: Hybrids mounted off-board
  - ◆ Analogue Cable -> Hybrid -> digital cable -> junction card -> twisted pair -> Adapter Card
- ❑ SVX4 chips mounted on hybrid; employed in SVX2 readout mode

# SVX4 Chip

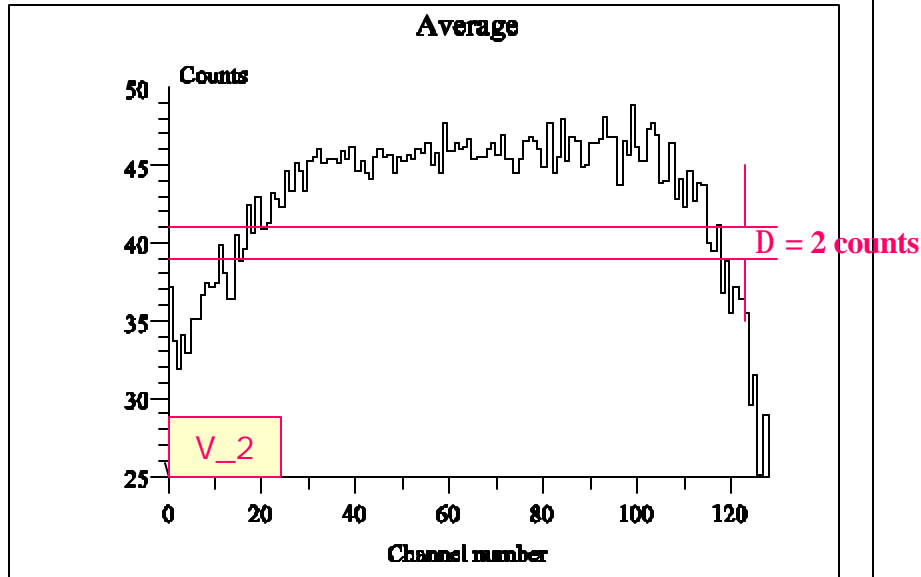
## □ SVX4 readout chip timeline

- ◆ Pre-amp (MOSI S 11/25/00)
- ◆ Pre-amp and pipeline (MOSI S 06/04/01)
- ◆ First full prototype received June 11, '02
  - Issues
    - few bugs
      - » pullup to USESEU.
      - » Add pullup or pulldown to DOMODE.
      - » Pull MSB of Chipl D high.
      - » Logic changes to FECLK gating/ADC control/FE control in D0Mode
    - features
      - » Large pedestal bow across chip
      - » channel to channel variation
      - » pedestal variation with pipeline depth
  - Redesign of comparator circuitry
  - Submitted to TSMC April '03
- ◆ Full preproduction chip received May 16, '03
  - 24 wafers, 454 chips/wafer; after yield ~ 3000 chips for CDF and DØ each
  - Initial tests demonstrate full functionality of the chip

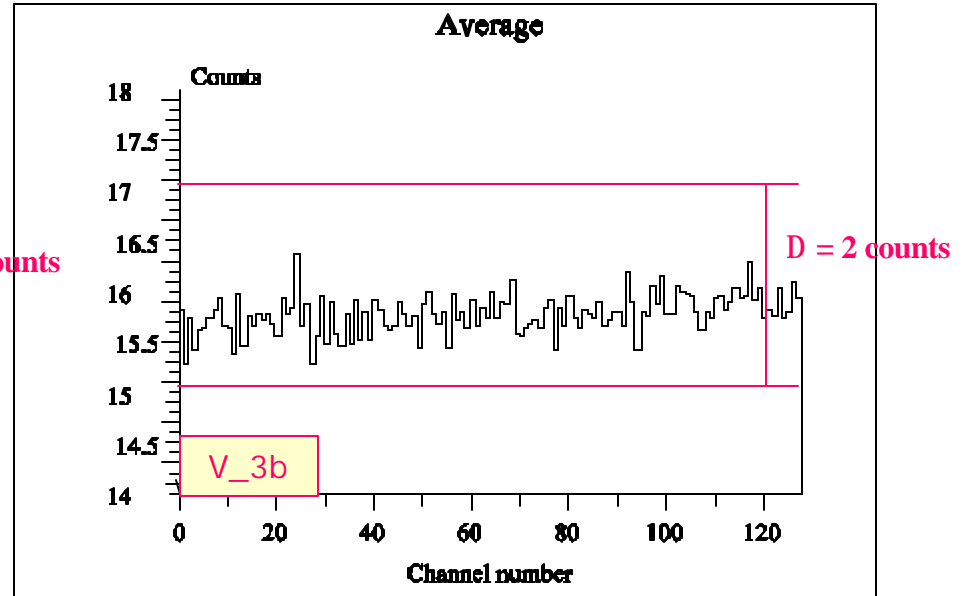


# SVX4 Chip

## □ Version 2 of chip (old)



## □ Initial result Version 3\_b (new)



- ◆ Bow structure in pedestal is gone even with extreme patterns and voltages
  - Minimize time between Comp. and ramp resets; Ramp Ped. set to max (lowest pedestal)
- ◆ Channel-to-channel fluctuations much smaller

## □ Testing plans

- ◆ Will test single chips asap at 14<sup>th</sup> floor (LBL and stimulus setups)
- ◆ Will stuff a few LO hybrids asap with untested chips
- ◆ Preparing a minimum list of tests to be performed on the chip

# Hybrids

## □ Layer 0

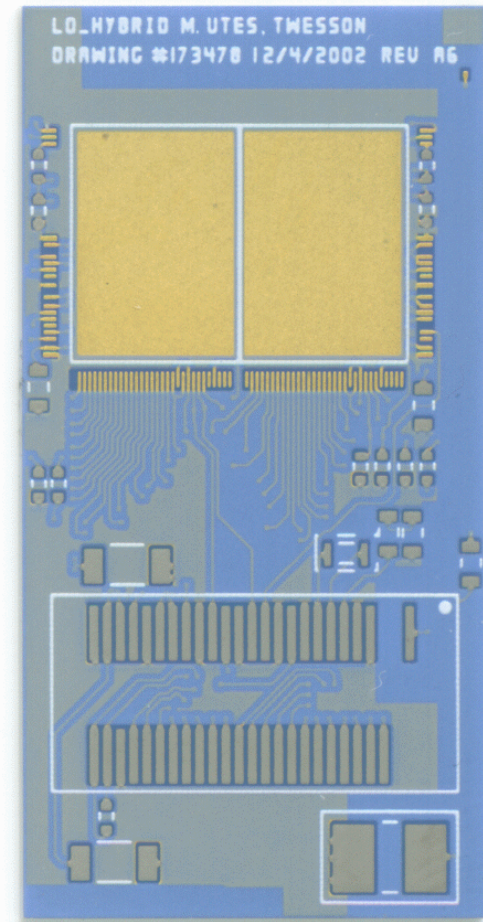
- ◆ 22 prototypes received from Amitron
  - Flatness 20-40  $\mu\text{m}$  (spec 100  $\mu\text{m}$ )
  - Thickness 750  $\mu\text{m}$  (spec 800  $\mu\text{m}$ )
- ◆ Hybrids rejected for mechanical reasons: crack in hybrid ~10 micron wide; not cross artwork; hybrid electrically ok
- ◆ Being used for L0 prototypes and works

## □ Layer 1

- ◆ 18 hybrids received from CPT (CA); 17 electrically good

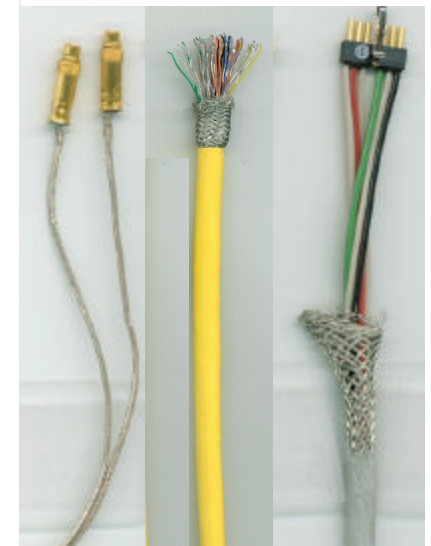
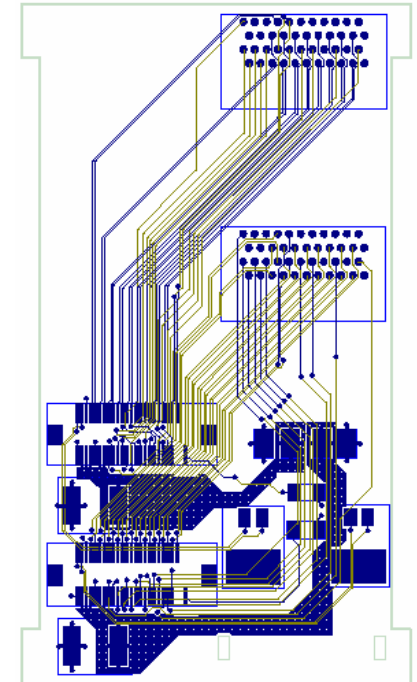
## □ Layer 2-5

- ◆ Received a total of 74 hybrids from Amitron and CPT
- ◆ Electrically all hybrids are ok; change in grounding for new rev.
- ◆ Mechanically hybrids have problems:
  - Flatness spec of 50  $\mu\text{m}$  not met by vendor
    - Not perfect CTE matching of BeO and dielectric causes bending during firing cycles; to compensate some dielectric is printed on the other side of BeO substrate
    - Limitation : Total thickness spec (0.95 mm) and processing issues
  - First three batches from CPT were close to the spec while two last batches failed
  - Flatness specification relaxed to 150  $\mu\text{m}$
- ◆ Revision of layout of hybrids completed May - June '03
- ◆ Order for new prototypes placed with 4 companies: CPT, Amitron, Halcyon, Scrantom



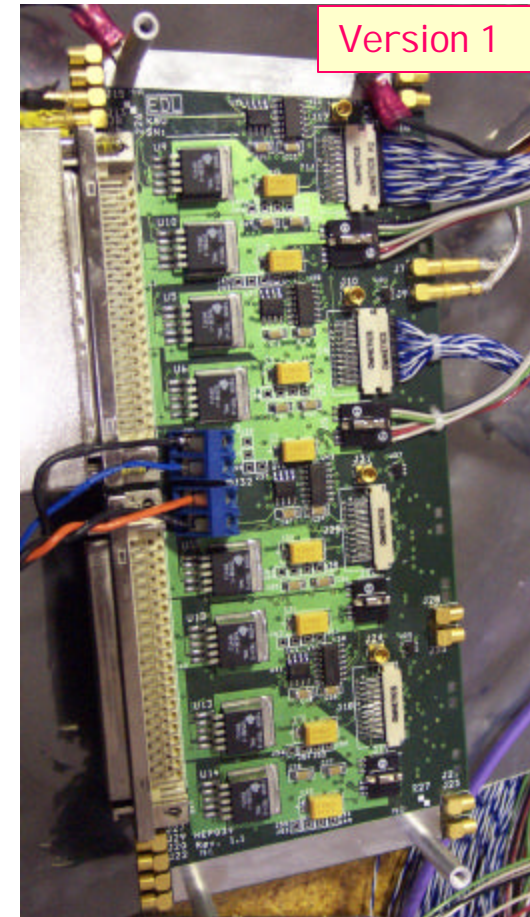
# Digital Cable, Junction Card and Twisted Pair

- ❑ DJC: Three vendors qualified
  - ◆ Honeywell, Basic Electronics, Century
- ❑ Ordered 450 test stand cables
  - ◆ Received 300 from Century; 150 ordered from Basic
  - ◆ Currently going through production steps
    - 150 cables : being ablated
    - 150 cables : AVX connectors installed, waiting for backing
- ❑ Junction card, no active elements
  - ◆ L0/1: 3 hybrids → 1 junction card
  - ◆ L2-5: 2 hybrids → 1 junction card, top/bottom
- ❑ Revised earlier design to accommodate installation
  - ◆ Receiving: 50-pin AVX connector away from z=0
  - ◆ Outgoing: soldered twisted pair cable bundle
- ❑ Twisted Pair
  - ◆ Power & HV lines : 6-pin Omnetics connector
  - ◆ Signal pairs : 44-pin Omnetics connector
  - ◆ Coax cables for clock signals
  - ◆ New prototype cable for New England Wire (common with CDF)
    - will use Omnetics connectors on both ends



# Adapter Card

- ❑ Active Card: interfaces new and existing readout electronics
  - ◆ Voltage regulation, SVX4 power
  - ◆ Differential-to-Single-Ended 2.5 to 5 V translation for SVX4 Data
  - ◆ 5 to 2.5 V translation for SVX4 Controls
  - ◆ Routing of Clock and HV
  - ◆ Each adapter card has four or six channels
    - Input: twisted pair
    - Output 80-conductor 3M cable (existing)
  - ◆ 12 boards fabricated
- ❑ Revision 2
  - ◆ Bypass clock lines on AC
  - ◆ Board power through 80C cable
  - ◆ One SVX4 power source, one voltage regulator/channel
  - ◆ Termination changes
  - ◆ Engineering review at KSU April '03
  - ◆ 12 boards to be fabricated by end of June



# Mechanical Issues Addressed

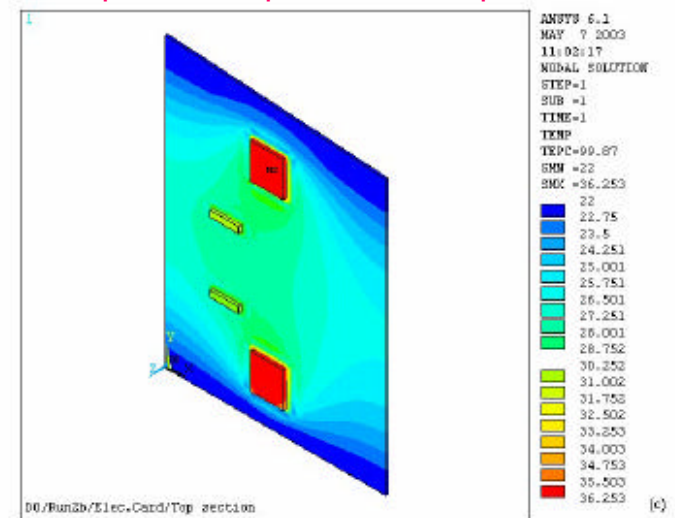
## ❑ Adapter Cards are mounted on face of calorimeter

- ◆ Four rings of adapter cards (dubbed the "horseshoe")
- ◆ Adapter card is now an active element and needs cooling, ~650W per side for read all mode, ~ 505W for sparse readout

## ❑ FEA analysis

- ◆ edges of card held at constant 22 °C
- ◆ transfer heat from AC to horseshoe through six standoffs
- ◆ 4 mil ground plane used for conductive cooling
- ◆ Maximum temperature of component is 36 °C.
  - hottest components on top
    - SVX4 power regulator
    - SVX4 single ended signal driver
  - hottest components on bottom
    - SVX4 bi-directional differential signal driver
    - Bi-directional drivers to IB
    - Board power regulators for 3.3V and 5V

Temperature profile on top side of AC



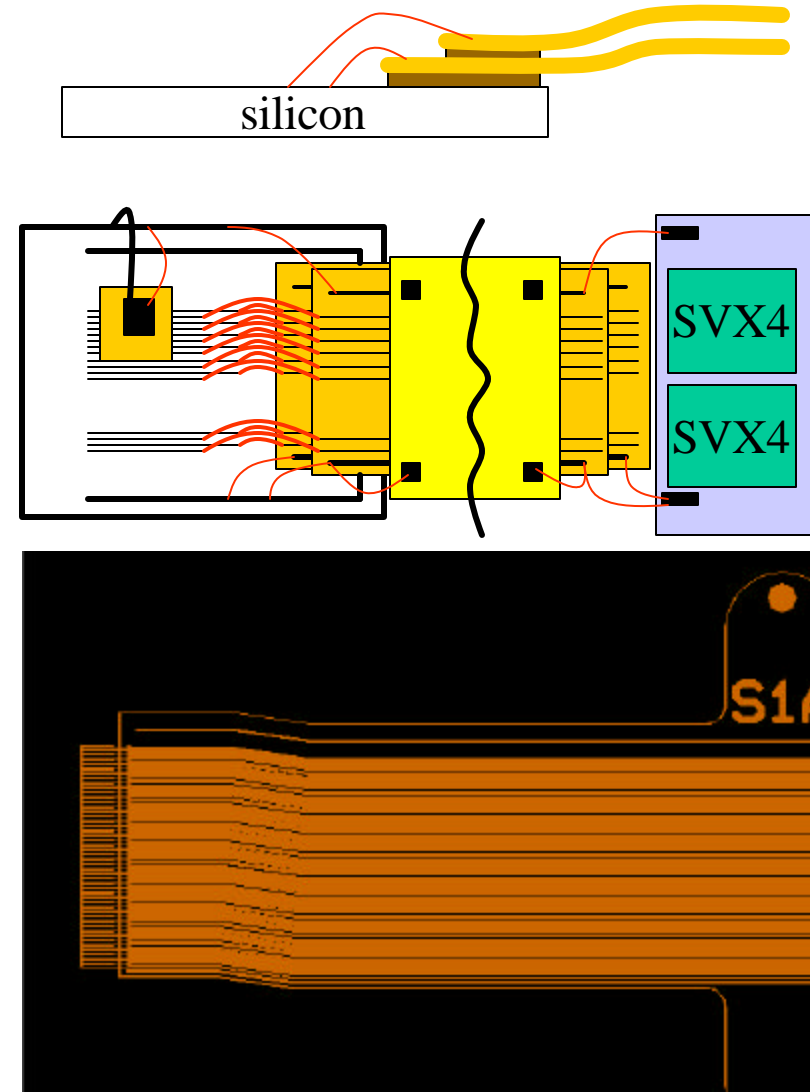
# Low Voltage Power Supply

- ❑ The LV power supply system needs to provide:
  - ◆ SVX4: 2.5V
  - ◆ Interface Board: +15V, 5V
  - ◆ Adapter Card: 5V (regulators and monitoring) and 3.3V (single ended drivers)
- ❑ PS will be located in MCH-1, needs long distance remote sense
- ❑ Two Wiener PS received in February '03
  - ◆ Power up and monitoring verified.
  - ◆ External interlock feature verified
  - ◆ Load test and regulation ongoing
  - ◆ CAN-bus to VME interface
    - The control/monitoring system under development
    - hardware in place, working on software issues.
    - Will be implemented at the two major integration tests (1% and 10% test stands)



# Analogue Flex Cables

- For layer 0 need low mass, fine pitch flex cables to carry analogue signals to hybrids
  - ◆ Technically challenging
    - **Trace width ~ 15 - 20 mm, pitch 91 mm**
    - **2 cables offset by 50 mm**
  - ◆ Noise determined by capacitance
    - For  $S/N > 10$ :  **$C < 0.55 \text{ pF/cm}$**
    - With 16mm trace width  $\rightarrow 0.51 \text{ pF/cm}$  for full cable assembly
- Fourth set of prototype cables (Dyconex)
  - ◆ 40 cables, max. length 463.65 mm
    - **No faults !**
    - **Mechanically and electrically cables of excellent quality**
- Remaining outstanding issue is bonding of cables with insertion of appropriate spacer and spacing material



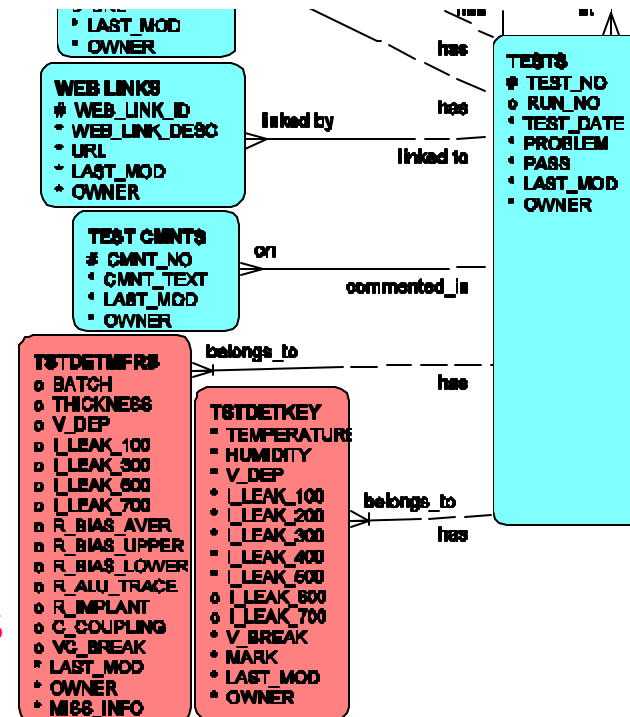
# Summary of Prototyping

Component	Vendor	First Prototype			Second Prototype			Final Order
		Design	Ordered	Delivered	Ordered	Delivered	Delivered	
L0 Sensors	HPK	✓						
L1 Sensors	HPK	✓	✓	✓				
L2 Sensors	HPK	✓	✓	✓				✓
Analogue Cable	Dycx	✓	✓	✓	✓	✓	✓	
L0 Hybrid	Amitr.	✓	✓	✓				
L1 Hybrid	CPT	✓	✓	✓				
L2A Hybrid	CPT	✓	✓	✓				
	Amitr.	✓	✓	✓				
L2S Hybrid	CPT	✓	✓	✓				
Digital Cable	Honey	✓	✓	✓	✓	✓	✓	
	Basic	✓	✓	✓	✓	✓	✓	
	Century	✓	✓	✓	✓	✓	✓	
Junction Card		✓	✓	✓	✓			
Twisted Pr. Cable		✓	✓	✓	✓		✓	
Adapter Card		✓	✓	✓				
Purple Card		✓	✓	✓	✓		✓	✓
Test Stand Elctr.		✓	✓	✓				✓

- Prototypes of all components in hand, no major issues anticipated; moving towards final (pre-)production orders

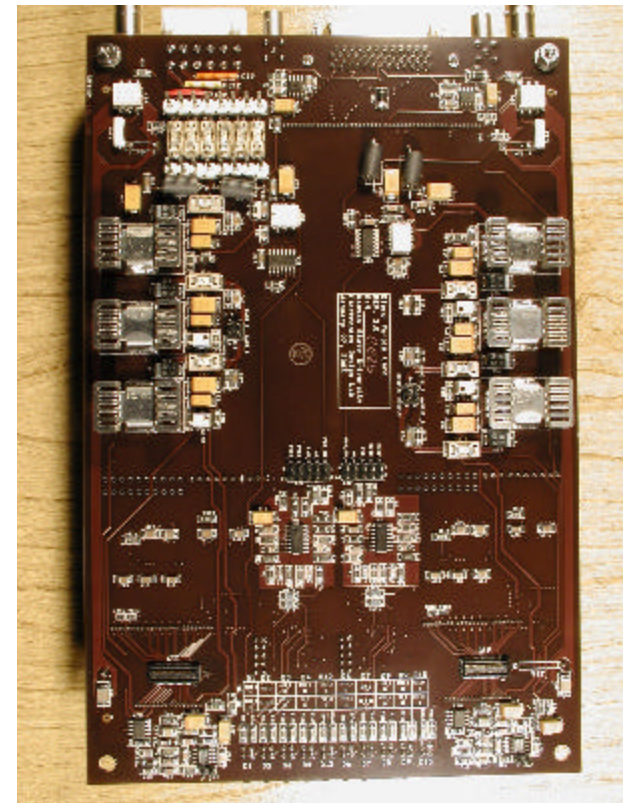
# Mapping and Software

- ❑ Map and crate assignments (VRB, Sequencer, I B) for detector complete
  - ◆ All references follow axial/stereo grouping
  - ◆ Respect STT requirements
  - ◆ Sequential Layer format chosen
- ❑ Software for data unpacking has been written
- ❑ Addressing scheme for modules, staves determined
  - ◆ L4-05NA-1010 (Layer 4,  $\phi$ -index 5, North, Axial, 10-10)
- ❑ Database
  - ◆ Switched from MySQL, university based database
  - ◆ Adopted ATLAS database design
    - Oracle based identity relationship
      - Item
      - Test
      - Assembly
      - Shipment/Tracking
    - Ideally suited to silicon detector
    - Supported by DØ online support group
    - Official transfer of designer files from ATLAS



# Testing: Burn-in Stands

- ❑ Components are rigorously tested in burn-in stands
  - ◆ Two hybrid burn-in test stands, 16 channels each
  - ◆ Two module burn-in test stands, 32 modules each
    - with associated cooling
  - ◆ Setup of burn-in stands complete at SiDet and passed Safety Inspection for 24/7 running
- ❑ Burn-in performed with stand-alone sequencer system and the 'Purple Card'
  - ◆ The equivalent of the "Adapter Card set" is a Purple Card
- ❑ Production Purple Cards received
  - ◆ 75 cards, 55 available, 20 still being debugged
  - ◆ After testing needs installation in burn-in stands
- ❑ Burn-in software: TclTk scripts
  - ◆ Runs for 4 chip hybrid; being extended for 6/10 chips
  - ◆ Tested for single SASEQ to be tested for multiple SASEQs
  - ◆ Most other functionality can be adopted from Run II a
  - ◆ As of Tuesday, ran successfully 1 hybrid for 3 days

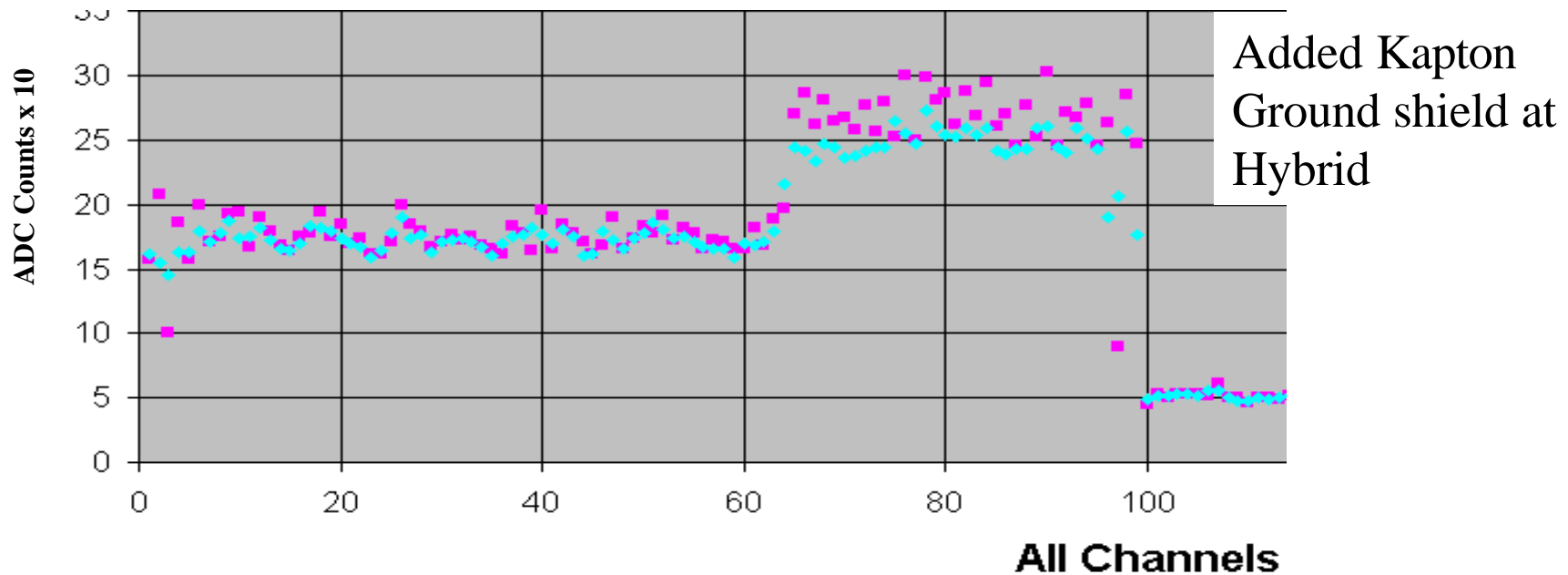


# Integration Tests

- Nearly all of the testing is performed with full system setups
  - ◆ Full Chain test with Stand-Alone sequencer
  - ◆ "1% Test"
    - Readout System at SiDet identical to the readout system used in the experiment
    - For functionality test of individual components up to a total of 8
    - setup complete and debugged; now being fully cabled
      - resolved incomplete readout for fraction of a percent of the events
  - ◆ "10% Test"
    - Readout System at SiDet identical to the readout system used in the experiment
    - Capability for full crate test; Tests planned:
      - Sector test of Layer 0
        - »  $3 \times 6 = 18$  hybrids, i.e. 3  $\phi$ -sectors; study noise with analogue cables
      - Sector test of Layer 1
        - »  $3 \times 6 = 18$  sensors, i.e. 3  $\phi$ -sectors; study and monitor operating conditions
      - Full sector test
        - » Minimum of 5 full staves readout, i.e. 20 hybrids
        - » Combination of Layer 0, Layer 1 and Staves
    - System currently being setup in the Lab C clean room at SiDet
  - ◆ In addition have laser setup and debugging stations

# Grounding for Inner Layers

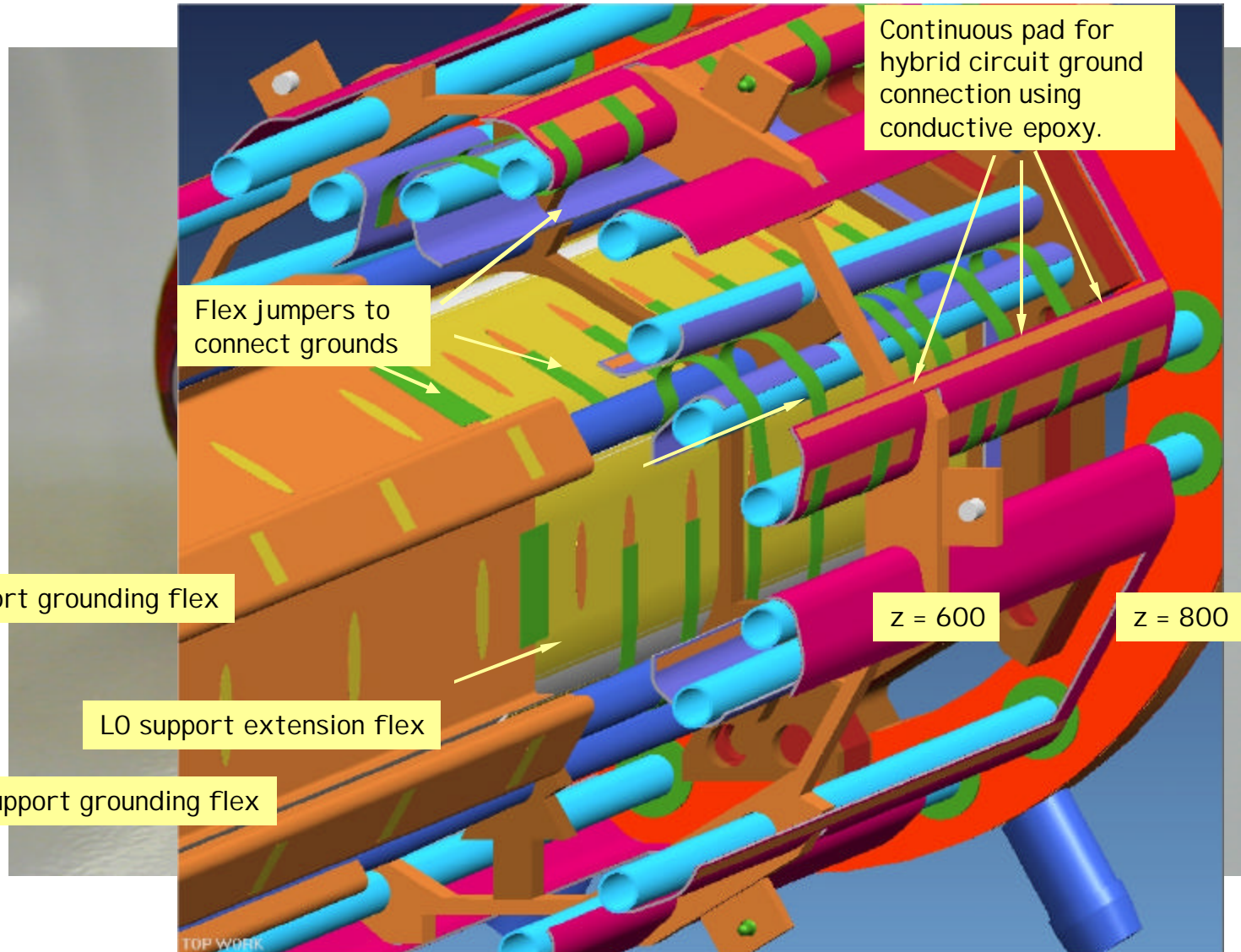
- ❑ Goal of  $S/N > 10$  for Layer 0 after irradiation
- ❑ Current results on the bench:
  - ◆  $S/N \sim 12$  before installation on support structure
  - ◆  $S/N \sim 11$  after installation in support structure



- ❑ Importance of providing low inductance ground connections and adequate overall grounding
- ❑ Studies ongoing to increase margin of  $S/N$

# Adopted Grounding Scheme

- 114+ flexible printed circuits will be implemented to address grounding for Layer 0



# Issues

- ❑ Overall schedule for completion of project slipped by 2.5 months compared to Lehman schedule (September '02)
  - Silicon Detector Complete: 9/12/05    Lehman
  - Silicon Detector Complete: 11/28/05    Now
  - ◆ Nearly all attributable to the SVX4 chip
  - ◆ However, we do have a working chip now which can be regarded as preproduction chip and signoff on various components can occur with current version of the chip
- ❑ Hybrids:
  - ◆ Vendors were not able to meet our flatness specification
  - ◆ Relaxed tolerance on flatness to 150  $\mu\text{m}$
  - ◆ Some vendors (CPT) have increased unit price by factor of 2 compared to budget
    - Started additional vendor qualification and contracted two new vendors
  - ◆ If SVX4 chips is indeed production version, hybrids will determine the critical path for the project
- ❑ Layer 0
  - ◆ S/N ratio currently obtained on the bench could be improved upon

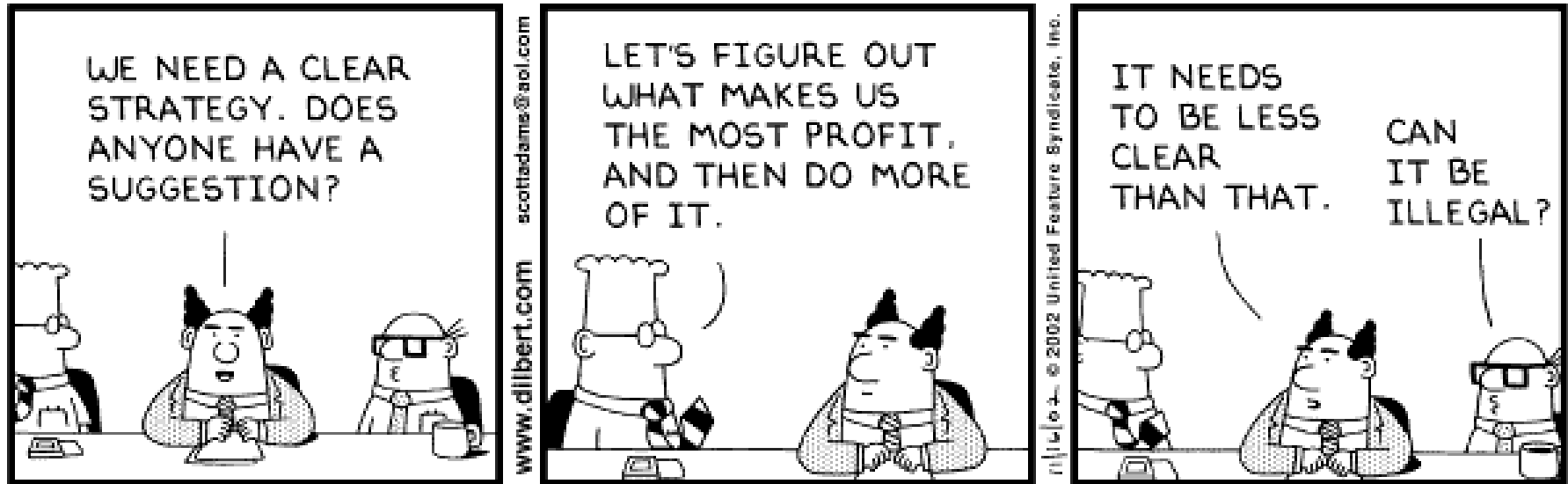
# Schedule

- Production Readiness Review is final step in signing off on design and releasing order

PRR for:	Scheduled Date	Comments
Purple Card	Jan 31 '03	All cards in hand
L2-5 Sensors <i>Done</i>	March 06, '03	Sensors to arrive in July
L0 & L1 Sensors	July '03	All documentation nearly ready
Low Voltage System	August '03	<i>This Fall</i>
High Voltage System	October '03	
L0 Hybrids	August '03	
L1 Hybrids	October '03	
L2-5 Hybrids	October '03	
Analogue Cables	September '03	
Digital Jumper Cables	October '03	
L0 & L1 Structures	Spetember '03	
Finalize Stave Design	August '03	
20 cm Gangs	September '03	
Junction Card	04	
Twisted Pair Cable	04	
Adapter Card	04	
Module Production	04	

- A very busy fall, but
  - ◆ no major technical difficulties foreseen
  - ◆ After this set of reviews nearly all elements are in production

# The Current Climate ?



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- ❑ We can only convince ourselves, management and the community with results and by performing well

# Summary and Conclusions

- ❑ Project has prototyped all components of the design
  - ◆ Remaining technical problems being addressed; don't seem to be major.
- ❑ We have started to place the final production orders for various components
- ❑ Project has a strong, knowledgeable, very dedicated team
- ❑ Whatever the future may hold for the Run I I b silicon project, it is not for lack of dedication of people within the collaboration!
- ❑ We will proceed, as in the past, and intend to continue building this detector as expeditiously as to not preclude a potentially very challenging and rewarding path for DØ and the HEP community as a whole; we are looking towards your continued support to accomplish this.